REMARKS/ARGUMENTS

Claims 1 – 9 are presented for reconsideration and further examination in view of the foregoing amendments and the following remarks.

In the outstanding Office Action, the Examiner indicated that claims 5 – 8 would be allowable if written in independent form; and rejected claims 1 – 4 and 9 under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art (hereinafter referred to as "AAPA") in view of U.S. Patent No. 5,388,022 to Ahuja (hereinafter referred to as "the Ahuja '022 patent").

By this Response and Amendment, headings have been added to the specification; claims 1 and 2 have been amended; and the Examiner's rejection has been traversed.

Applicant respectfully submits that the no new matter, within the meaning of 35 U.S.C. §132, has been introduced.

Claim Rejection Under 35 USC 103

The Examiner rejected claims 1 – 4 and 9 as being unpatentable over AAPA in view of the Ahuja '022 patent.

Response

Applicant respectfully traverses the Examiner's rejection since all of the features of the presently claimed invention are not disclosed, taught or suggested in the cited prior art.

Independent claim 1 recites "[a] residual current detection circuit comprising means for detecting an imbalance current indicative of a residual current and providing an output whose amplitude corresponds to the magnitude of the residual current, the output being applied

simultaneously to two channels wherein the first channel provides a first signal and the second channel provides a second signal whose onset is time delayed with respect to the onset of the first signal, the output of each channel being applied to a circuit stage which produces an output only when the first and second signals are coincident at its input whereby *the circuit stage produces an output only if the duration of the first signal is greater than the delay in the onset of the second signal.*" Independent claim 2 also recites that "the output signal is provided only if the duration of the first signal is greater than the delay in the onset of the second signal."

AAPA discloses a residual current detection circuit; however, it does not disclose, teach or suggest a circuit breaker with an AND gate that is able to output a signal when simultaneous signals are present. The Examiner combines the Ahuja '022 patent with the Background section of the originally filed specification to render the presently claimed invention obvious. The Ahuja '022 patent discloses an auto-reset circuit breaker having a current sensing device that opens the circuit for a defined delay interval in response to an overage in current. In other words, it is the increased current that triggers a delay mechanism.

Generally, in contrast to the cited combination of prior art, independent claim 1 recites that "the circuit stage produces an output *only* if the duration of the first signal is greater than the delay in the onset of the second signal" and independent claim 2 recites that "the output signal is provided only if the duration of the first signal is greater than the delay in the onset of the second signal." The second signal is delayed with respect to the first regardless of the amount of current in the circuit. With the Ahuja '022 patent, time delay and the output of the AND gate is determined by whether there is a current overage in the circuit.

Specifically, as stated in the specification, the object of the present invention is to avoid

or reduce the incidence of nuisance tripping caused, for example, by very short high amplitude voltage spikes or noise bursts on the mains supply. This is achieved by applying the detected signal to first and second channels and effectively ANDing the outputs of the channels. However, the signal in the second channel is delayed relative to the signal in the first channel, so that a "trip" signal is only produced if the signals in the two channels are coincident at the AND circuit. The onset of the signal in the second channel should be delayed relative to the onset of the signal in the first channel, as clearly described in the paragraph starting on page 6, line 8 of the originally filed specification. The trip signal is only produced if the duration of the signal in the first channel is greater than the delay in the onset of the signal in the second channel.

This relationship does not exist in the circuit disclosed in Ahuja. Referring to col. 3, lines 25 – 68 and related Figures 1 and 1(a) to 1(d), the signal at the output 25 of the comparator and control circuit 22, i.e. the circuit that determines whether there is an over-voltage or over-current condition, is shown in Figure 1(c) and corresponds to the over-current condition shown in Figure 1(a). Note that the normal output of the circuit 22 is high and goes low when an over-voltage or over-current condition is detected – compare Figures 1(a) and 1(c). Thus, in Figures 1(b) to 1(d), the negative-going regions of the waveforms constitute the meaningful signals.

It will therefore be seen by comparing the waveforms in Figures 1(c) and 1(d) that the signal produced by the time delay 26, and whose waveform is shown in Figure 1(d), is only delayed *at its end* relative to the signal at 25, and its onset is coincident with the onset of the undelayed signal in Figure 1(c). In fact, all that the time delay 26 does is to lengthen the negative-going pulse in Figure 1(c).

Contrastingly, in the presently claimed invention, the delay period is used to delay the

response to the occurrence of an event. In the Ahuja '022 patent circuit, the response of the circuit is instantaneous and the delay is used to maintain the response for a determined period. In effect, the delay in the presently claimed invention is a precondition to an outcome whereas in the Ahuja circuit it is a post condition to an outcome.

It is also pointed out that, since the solid state switch 16 of Ahuja opens if either one of the negative-going delayed and undelayed signals, Figures 1(c) and 1(d), is present at the inputs of the AND gate 30, the latter is actually operating as an OR gate in respect of these signals. In other words a trip signal, Figure 1(b), is provided if either one of the negative-going delayed or undelayed signals is present at the AND gate. This is contrary to claim 1, which recites "a circuit stage which produces an output only when the first and second signals are coincident at its input" and to claim 2, which recites "means for providing an output signal only when the first signal is coincident with the second signal" where a trip signal is only produced when there is coincidence between the delayed and undelayed signals.

Accordingly, the Ahuja circuit, if used in combination with the AAPA, would do nothing to mitigate the incidence of nuisance tripping and in fact would tend to exacerbate the situation by prolonging the response period. Therefore, the presently claimed invention is not rendered obvious by the prior art combination.

In the light of the foregoing Applicant submits that the claims are patentably distinguished over the cited art. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection.

CONCLUSION

In light of the foregoing, Applicant submits that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not timely filed, Applicant petitions for an appropriate extension of time. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 14-0112.

Respectfully submitted,
NATH & ASSOCIATES PLLC

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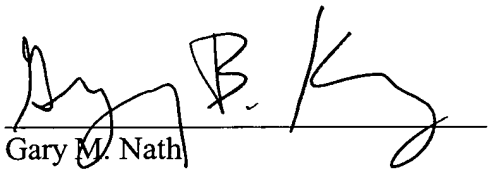
By: 

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